

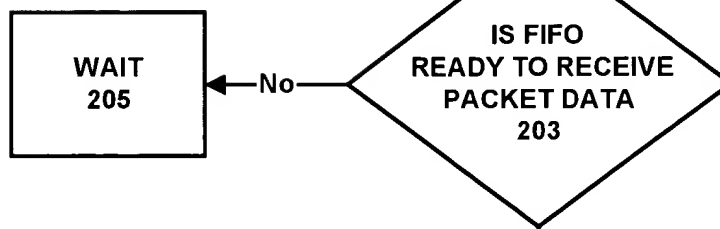
FIG. 1 is a block diagram of a data transfer system. The system includes a CPU 100, a North Bridge 102, a Memory 101, a Memory Bus 103, a CPU 100, a South Bridge 112, a DVD Source 114, a FIFO 110, a Decoder 118, and various signal lines (Data 130, Valid 132, Clock 134, Write Enable 120, Refill Interrupt 122, PCI Bus 105).

The CPU 100 is connected to the North Bridge 102. The North Bridge 102 is connected to the Memory 101 (which contains DRAM 104, DRAM 106, and DRAM 108) via the Memory Bus 103. The North Bridge 102 is also connected to the CPU 100 via the Memory Bus 103. The North Bridge 102 is connected to the South Bridge 112 via the PCI Bus 105. The South Bridge 112 is connected to the DVD Source 114. The North Bridge 102 is connected to the FIFO 110 via the Write Enable 120 and the Refill Interrupt 122. The FIFO 110 is connected to the Decoder 118 via the Data Signal Line 130, the Valid Signal Line 132, and the Clock Signal Line 134. The FIFO 110 is also connected to the DVD Source 114 via the Clock Signal Line 134.

# FIG. 1

READ DVD DATA ACROSS  
PCI BUS  
200

DECRYPT DVD DATA AND  
CREATE PACKET DATA  
202



SEND PACKET DATA TO  
FIFO VIA NORTH BRIDGE  
AND MEMORY BUS  
204

FORWARD PACKET DATA  
FROM FIFO TO MPEG  
DECODER VIA TRANSPORT  
BUS  
206

DECODE PACKET DATA  
AND PRODUCE MPEG DATA  
STREAM  
208

FIG. 2